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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/929,150 | 08/13/2001 | Jyh-Ming Jong | SUN-P5887-RJL | 8924 |

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| EXAMINER | |
|---|---|
| BELLO, AGUSTIN | |
| **ART UNIT** | **PAPER NUMBER** |
| 2633 | |

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/929,150 | JONG ET AL. | |
| | Examiner | Art Unit | |
| | Agustin Bello | 2633 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/19/04, 11/25/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS FILED 8/13/02*.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 2, 3, 12, 13, 21, and 22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicant claims that the phase-lock-loop generates a plurality of clock signals that have a frequency that is higher than the frequency of the reference clock signal. However, the examiner can not find any disclosure of this feature in the specification. At most, the applicant discloses that the frequency of the clock signals generated by the phase-lock-loop is "approximately *equal* to the frequency of the first electrical signal 315" page 8 lines 5-12 in the specification.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art admitted by the applicant (Figure 2) in view of Hendrickson (U.S. Patent Application Publication No. 2002/0093994).

Regarding claim 1, the prior art admitted by the applicant teaches a first photo-detector (reference numeral 235 in Figure 2), the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal (reference numeral 215 in Figure 2); a phase-locked-loop (reference numeral 205 in Figure 2), the phase-locked-loop operable to receive a reference clock signal (reference numeral 210 in Figure 2); a clock-recovery circuit (reference numeral 220 in Figure 2), the clock-recovery circuit coupled to the phase-locked-loop (reference numeral 205 in Figure 2), the clock-recovery circuit operable to receive the first electrical signal (as seen in Figure 2); a first latch-decision circuit (reference numeral 225 in Figure 2), the first latch-decision circuit coupled to the clock-recovery circuit (reference numeral 220 in Figure 2); a first latch (reference numeral 230 in Figure 2), the first latch coupled to the first latch-decision circuit (reference numeral 225 in Figure 2), the first latch operable to receive the first electrical signal (reference numeral 215 in Figure 2); a second photo-detector (reference numeral 265 in Figure 2) the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal (reference numeral 245 in Figure 2); a second latch-decision circuit (reference numeral 255 in Figure 2); and a second latch (reference numeral 260 in Figure 2), the second latch coupled to the second latch-decision circuit (reference numeral 255 in Figure 2), the second latch operable to receive the second electrical signal (reference numeral 245 in Figure 2). The prior art differs from the claimed invention in that prior art fails to specifically teach that the second latch-decision circuit coupled to the clock-

recovery circuit. However, coupling a plurality of latches to a single clock-recovery circuit is well known in the art. Hendrickson, in the same field of optical receivers, teaches coupling a plurality of latches to a single clock recovery circuit (Figure 14). One skilled in the art would have been motivated to couple a plurality of latches to a single clock-recovery circuit in order to reduce the overall complexity and expense of the receiver circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to couple a plurality of latches to a single clock-recovery circuit as taught by Hendrickson.

Regarding claims 3 and 13, the prior art admitted by the applicant and Hendrickson teach that at least one at least one of the plurality of clock signals has a phase that is not equal to the phase of the reference clock signal (page 2 lines 8-15 of the applicant's specification and paragraph 0068 of Hendrickson).

Regarding claims 4 and 14, the prior art admitted by the applicant teaches that the clock-recovery circuit is operable to extract timing information from the first electrical signal (page 2 lines 18-20 of the specification).

Regarding claims 5 and 15, the prior art admitted by the applicant teaches he first latch-decision circuit, based upon timing information received from the clock-recovery circuit, is operable to determine a time to latch the first electrical signal (page 3 lines 1-5 of the specification).

Regarding claim 6 and 16, the prior art admitted by the applicant teaches that the first latch-decision circuit (reference numeral 225 in Figure 2) is operable to receive the first electrical signal (reference numeral 215 in Figure 2).

Regarding claim 7, the prior art admitted by the applicant teaches that the first latch-decision circuit (reference numeral 225 in Figure 2) is operable to receive the first electrical signal (reference numeral 215 in Figure 2) and the second latch-decision circuit (reference numeral 255 in Figure 2) is operable to receive the second electrical signal (reference numeral 245 in Figure 2),

Regarding claims 8 and 17 the prior art admitted by the applicant teaches that the first latch-decision circuit (reference numeral 225 in Figure 2) is operable to receive the first electrical signal (reference numeral 215 in Figure 2) and, based upon information extracted from the first electrical signal and timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal (page 3 lines 1-5 of the specification).

Regarding claims 9 and 18, the prior art admitted by the applicant teaches that the first photodetector includes a photodiode (page 2 line 5 of the specification).

Regarding claims 10 and 19, the prior art admitted by the applicant teaches the first photo-detector is operable to receive an optical signal that is compliant with an optical signal defined in the InfiniBand specification (page 3 lines 15-18 of the specification).

Regarding claim 11, the prior art admitted by the applicant teaches a first photo-detector (reference numeral 235 in Figure 2), the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal (reference numeral 215 in Figure 2), a phase-locked-loop (reference numeral 205 in Figure 2), the phase-locked-loop operable to receive a reference clock signal (reference numeral 210 in Figure 2); a clock-recovery circuit (reference numeral 220 in Figure 2), the clock-recovery circuit coupled to the phase-locked-loop (reference numeral 205 in Figure 2), the clock-recovery circuit operable to receive the first

electrical signal (reference numeral 215 in Figure 2); a latch-decision circuit (reference numeral 225 in Figure 2), the latch-decision circuit coupled to the clock-recovery circuit (reference numeral 220 in Figure 2), a first latch (reference numeral 230 in Figure 2), the first latch coupled to the latch-decision circuit (reference numeral 225 in Figure 2), the first latch operable to receive the first electrical signal (reference numeral 215 in Figure 2); a second photo-detector (reference numeral 265 in Figure 2), the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal (reference numeral 245 in Figure 2); and a second latch (reference numeral 260 in Figure 2, the second latch operable to receive the second electrical signal (reference numeral 245 in Figure 2). The prior art admitted by the applicant differs from the claimed invention in that it fails to specifically teach that the second latch coupled to the latch-decision circuit. However, Hendrickson in the same filed of optical receivers teaches it is well known in the art to couple a plurality of latches to a single latch-decision circuit (e.g. selectors 203/209 coupled to latches 201/205/211). One skilled in the art would have been motivated to couple a plurality of latches to a single latch decision circuit in order to reduce the overall cost and complexity of the receiver circuit. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to couple a plurality of latches to a single latch decision circuit as taught by Hendrickson.

5. Claims 20-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over the prior art admitted by the applicant (Figure 2) in view of Wijntjes (U.S. Patent No. 6,718,143).

Regarding claim 20, the prior art admitted by the applicant teaches a first photo-detector (reference numeral 235 in Figure 2), the first photo-detector operable to receive the first input data signal and operable to output a first electrical signal (reference numeral 215 in Figure 2); a

second photo-detector (reference numeral 265 in Figure 2), the second photo-detector operable to receive the second input data signal and operable to output a second electrical signal (reference numeral 245 in Figure 2); a phase-locked-loop (reference numeral 205 in Figure 2), the phase-locked-loop operable to receive a reference clock signal (reference numeral 210 in Figure 2); a clock-recovery circuit (reference numeral 220 in Figure 2), the clock-recovery circuit coupled to the phase-locked-loop, the clock-recovery circuit operable to receive the first electrical signal (reference numeral 215 in Figure 2); a latch-decision circuit (reference numeral 225 in Figure 2), the latch-decision circuit coupled to the clock-recovery circuit (reference numeral 220 in Figure 2); and a latch (reference numeral 230 in Figure 2), the latch coupled to the latch-decision circuit (reference numeral 225 in Figure 2). The prior art admitted by the applicant differs from the claimed invention in that it fails to specifically teach that the latch is operable to receive the first electrical signal and the second electrical signal. However, single latch units are well known in the art. Wijntjes, in the same field of endeavor, teaches it is well known that single latch units which receive a plurality of inputs are well known in the art (see "LATCH" in Figure 3). One skilled in the art would have been motivated to include a single latch unit as taught by Wijntjes in the device of the prior art admitted by the applicant in order to reduce the overall cost and complexity of the receiver. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to use a single latch as taught by Wijntjes in the device of the prior art admitted by the applicant.

Regarding claim 22, the prior art admitted by the applicant and Hendrickson teach that at least one at least one of the plurality of clock signals has a phase that is not equal to the phase of

the reference clock signal (page 2 lines 8-15 of the applicant's specification and paragraph 0068 of Hendrickson).

Regarding claim 23, the prior art admitted by the applicant teaches that the clock-recovery circuit is operable to extract timing information from the first electrical signal (page 2 lines 18-20 of the specification).

Regarding claim 24, the prior art admitted by the applicant teaches he first latch-decision circuit, based upon timing information received from the clock-recovery circuit, is operable to determine a time to latch the first electrical signal (page 3 lines 1-5 of the specification).

Regarding claim 25, the prior art admitted by the applicant teaches that the first latch-decision circuit (reference numeral 225 in Figure 2) is operable to receive the first electrical signal (reference numeral 215 in Figure 2).

Regarding claim 26, the prior art admitted by the applicant teaches that the first latch-decision circuit (reference numeral 225 in Figure 2) is operable to receive the first electrical signal (reference numeral 215 in Figure 2) and, based upon information extracted from the first electrical signal and timing information received from the clock-recovery circuit, is operable to determine a time to latch the first input signal (page 3 lines 1-5 of the specification).

Regarding claim 27, the prior art admitted by the applicant teaches that the first photodetector includes a photodiode (page 2 line 5 of the specification).

Regarding claim 28, the prior art admitted by the applicant teaches the first photo-detector is operable to receive an optical signal that is compliant with an optical signal defined in the InfiniBand specification (page 3 lines 15-18 of the specification).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Agustin Bello whose telephone number is (571) 272-3026. The examiner can normally be reached on M-F 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on (571)272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Agustin Bello
Examiner
Art Unit 2633

AB

JASON CHAN
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